Via Currents and Temperatures

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For a complete analysis of trace and via currents and temperatures, see Brooks and Adam, ***PCB Trace and Via Currents and Temperatures: The Complete Analysis,*** *Available at Amazon.com, https://www.amazon.com/PCB-Trace-Via-Currents-Temperatures/dp/1530389437/ref=la_B001IR1JBS_1_4?s=books&ie=UTF8&qid=1476216597&sr=1-4*

In two previous papers [1] the authors explored the current/temperature relationships of PCB traces under normal current loads and under a significant overload of what would be considered the normal current carrying capacity of the trace ("fusing" current and time.) But through the years there has been very little written about the current carrying capacity of a via.

A via typically has a drill diameter and a copper conducting thickness formed during a plating process. This gives the via a conducting cross-sectional area. Consider the situation where a via connects a plane or trace on one layer to a plane or trace on another layer. If that via will carry a significant current (i.e. a current high enough to heat a trace to some degree), how big do we need to make the via's cross-sectional area [2] in order to safely handle that current? Until now there is been very little practical guidance on that question. In this article the authors provide an answer based on a thermal simulation tool called TRM (Thermal Risk Management.)[3]

Board designers typically approach this question using one of three strategies:

1. Simply don't allow vias that carry higher levels of current. Route all the conductors on the same trace layer.
2. Size the via to handle the current using the IPC 2152 [4] guidelines.
3. Use a "standard" via known to be able to carry a certain amount of current and use multiple vias in parallel, as many as needed for the total current carried by the trace.

IPC 2152 explicitly endorses 2 and/or 3 on page 26:

> *The cross-sectional area of a via should have at least the same cross-sectional area as the conductor or be larger than the conductor coming into it. If the via has less cross-sectional area than the conductor, then multiple vias can be used to maintain the same cross-sectional area as the conductor.*

Anecdotally this must be good advice because most designers have never had a via fail for purely thermal reasons (unless there was a fabrication or alignment issue.) What we have been doing must be right, because it works so well! In fact, we will show in this paper that this guidance has been *extremely* conservative.

But there is an implicit assumption in this guidance that sometimes poses a problem. That is, it is assumed we know the plating thickness of the via. We typically assume (*hope* might be a better word) that the via wall thickness is the same as the plating thickness, which is typically 0.5 or 1.0 Oz. copper (0.65 to 1.3 mils). But the plating is often not uniform on the walls of the via. This is a separate problem that we are not prepared to address in this paper.

Assumptions and Strategies:

So we are going to proceed with the following set of assumptions and strategies:

1. We will assume a standard via with a 10 mil (0.26 mm) drill diameter and a 0.030 mm uniform plating thickness. This is slightly less than a 1.0 Oz equivalent. The effective cross-sectional area of this via is $\pi(r^2 - (r\text{-}th)^2)$ where r is the via radius and th is the plating thickness. Choosing these mm equivalents (which are slightly rounded) results in a via cross-sectional area of .0217 mm^2. This is approximately equivalent to a 1 Oz. 26 mil (.66 mm) wide trace [5].

2. The pad area of a via doesn't matter because we are going to be dealing with traces that are at least 26 mils (0.66 mm) wide. (If we were dealing with smaller traces, the via cross-sectional area would exceed that of the trace and should be OK from a heating standpoint "by definition.")

3. We will be dealing primarily with a standard board thickness of 63 mils (1.6 mm).

4. We will vary the trace width and current and compare the temperature of the trace on the board with the via temperature. In this way, we will see if the via gets hotter than the trace, stays the same temperature as the trace, or runs cooler than the trace.

5. We assume that at low currents via temperature is not a problem. Since we are primarily concerned with high-temperature effects, we will concentrate on what happens at higher temperatures and currents.

Thermal Model:

Our thermal model is a pair of 60 mm long traces on either side of a board connected by a 0.26 mm diameter, 0.03 mm plated via. The board is a few mm wider than the trace. The dielectric layer between the trace layers is 1.6 mm FR4. A thermocouple (TC in Figure 1) is placed near the midpoint of the top trace. This will measure the temperature at that point during the simulations. The purpose for this will be described later. A diagram of this model is shown in Figure 1.

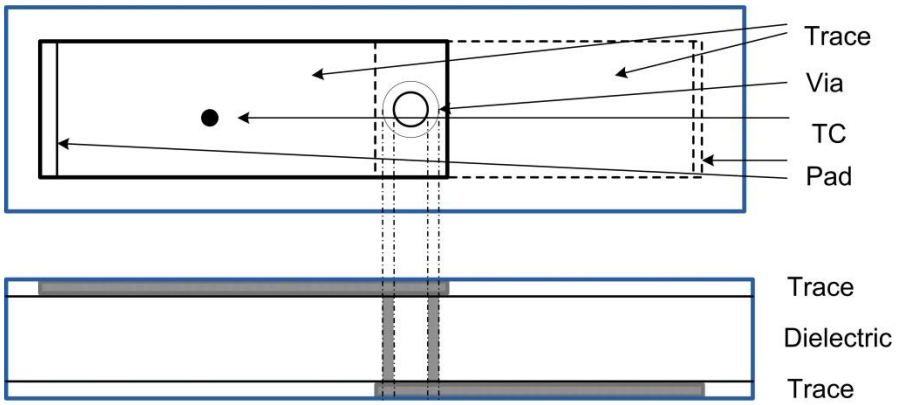

Figure 1
Thermal model of trace with via. *(Not to scale)*

First Simulation:

Our first series of simulations will be run with this model in five widths, 0.40 mm, 0.66 mm, 1.2 mm, 1.8 mm, and 2.5 mm. (This approximately corresponds to widths of 26 mil, 47 mil, 71 mil and 100 mil, respectively.) The results of the first simulation, 0.66 mm, are shown in Table 1. The values shown are the temperatures (NOT the temperature *change*) at the thermocouple (TC), the maximum temperature point of the upper trace, the midpoint of the via, and the "Bare trace."

Table 1

Temperatures in the Simulation at Various Points and Currents				
Current (A)	TC	Via top	Via midpoint	Bare Trace
3	86.9	81.4	80.9	86.2
4	166.7	154.1	152.9	165.0

One of the first questions to ask about the simulation temperatures is "compared to what?" We also modeled each configuration as a single trace (bare trace) on a single layer with no via, under the same conditions. This way we can compare the via temperatures with what the trace temperature would be without the via. The thermocouple (TC) was intended to provide this information. The "Bare Trace" temperature is a check on that assumption. In every simulation the "Bare Trace" temperature was nearly identical to the TC temperature, normally differing by significantly less than one degree C. Only above 100 degrees C did the difference approach or slightly exceed 1.0 degree C.

In this first simulation, the via cross-sectional area and the trace cross-sectional area are the same. Under the assumption that the cross-sectional area of the via determines the via temperature, the via midpoint temperature should equal the same as the TC (which equals the temperature of a "bare trace" without a via.) We can see from Table 1 that *this is not true*. At 3 Amps the via runs approximately 7 degrees C *cooler* than the trace and at 4 Amps it runs approximately 14 degrees C *cooler*. The thermal profile of the top trace layer at 3 Amps is shown in Figure 2. It is apparent that the trace begins to *cool* as approaches the via in the center.

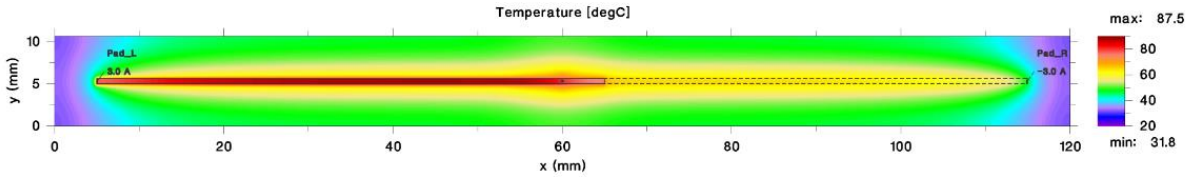

Figure 2

Thermal profile of the top trace layer of the first simulation at 3 Amps.

The reason for this has not been obvious up until now. One of the surprises in IPC 2152 is that internal traces run somewhat cooler than do external traces of the same dimension. That is because, it turns out, the heat spreading through the dielectric supports more cooling than does convection and radiation into the air. The via looks very similar to an internal trace surrounded by a dielectric. That is why it runs cooler than an equivalent trace on the top layer. Furthermore, the copper is an extremely good conductor of heat. The via and the trace have the same cross-sectional area, and therefore the same resistance per-unit-length. Therefore, we can expect them both to heat approximately equally through the I^2R heating mechanism. Since the via runs cooler than the trace, what is happening is that *the via is helping to cool the trace*.

The results of the first simulation are shown graphically in Figure 3. In these graphs the via midpoint temperatures are shown in red and the TC temperatures are shown in black. All traces are assumed to "start" at 20 degrees C at 0.0 Amps.

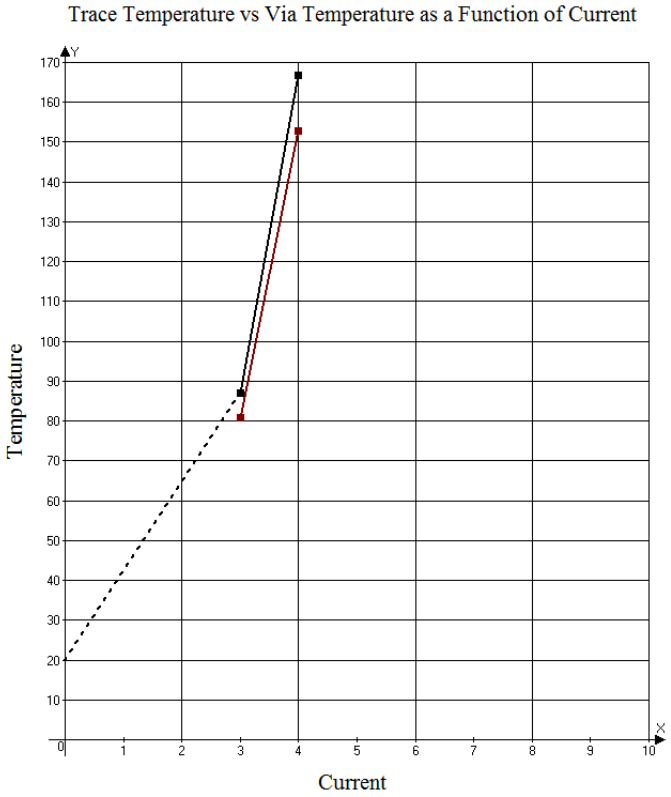

Figure 3

Via and trace temperature vs. current for a 0.66 mm wide 1.0 Oz. trace.

Additional Simulations:

We ran additional simulations at three other widths. The results are shown in Table 2, and graphed in Figure 4. The graph sets from left to right are for 1.2 mm, 1.8 mm, and 2.5 mm traces respectively (approximately 47 mil, 71 mil, and 100 mil.)

Table 2

Temperatures in the Simulation at Various Points and Currents				
Width (mm)	Current (A)	TC	Via top	Via Midpoint
0.4	2	91.4	83.2	82.4
0.4	2.3	123.2	111.1	109.9
0.66	3	86.9	80.9	86.2
0.66	4	166.7	152.9	165.0
1.2	3	47.9	48.6	48.7
1.2	4	74.1	75.7	75.8
1.2	5	115.5	118.75	118.75
1.8	5	70.8	76.8	76.8
1.8	6	100.2	110.2	110.2
2.5	6	68.1	77.6	77.6
2.5	7	90.3	104.9	104.9

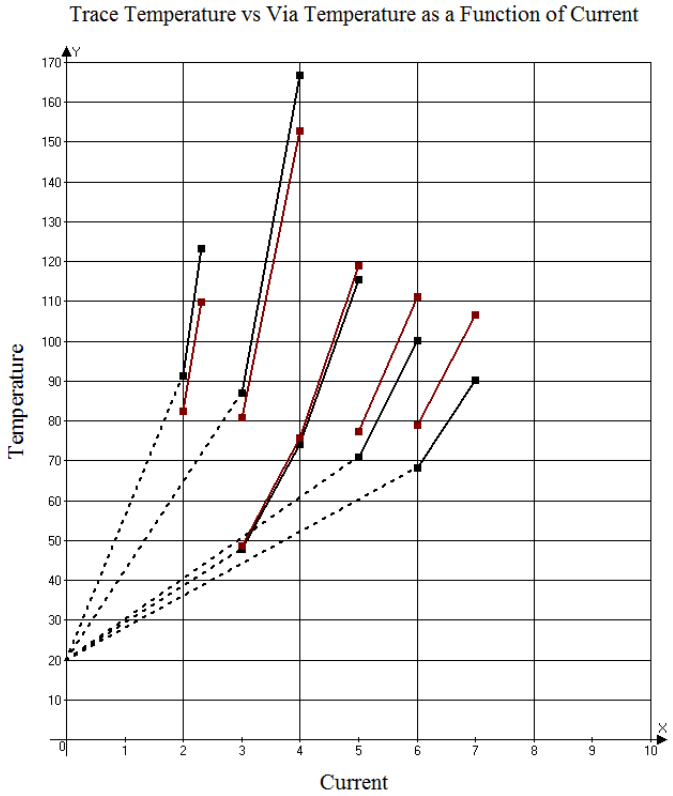

Figure 4

Via and trace temperature vs. current for selected widths.

At a 1.2 mm trace width, about twice the cross-sectional area of the via, the via temperature is about the same as the trace temperature at any current level. As the trace width increases, and as the current

increases, the via does start running a little hotter than the trace, but only by a few degrees. As the trace width gets wider, and therefore can handle the thermal heating better than the via can, the trace starts cooling the via (because of the high thermal conductivity between the via and the trace.) For example, look at the comparison in Table 3.

Table 3

Temperatures in the Simulation at Various Points and Currents				
Width (mm)	Current (A)	TC	Via top	Via Midpoint
.04	2	91.4	83.2	82.4
0.66	3	86.9	81.4	80.9
1.2	4	74.1	75.7	75.8
1.8	5	70.8	76.8	76.8
2.5	6	68.1	77.6	77.6

The via cross-sectional area is about the same as that for a 0.66 mm trace. Under the old guidelines, we would expect the via temperature to increase with current. But the via midpoint temperature stays approximately the same as we increase the current and the trace width at the same time. At 6.0 Amps the via is running *cooler* with a 2.5 mm trace than it does at 3 Amps with a 0.66 mm trace!

The comparison is even more dramatic if we simulate a 2 Oz. trace. Just for fun, we look at a 2.5 mm, 2 Oz. trace carrying 7 and 10 Amps with only a single via. The results are shown in Table 4. Note that with 10 Amps the via midpoint temperature is about 118 degrees C, almost 25 degrees hotter than the trace TC. But consider this: a single 0.66 mm trace (with the same cross-sectional area as this via) carrying 10 Amps would reach the melting point of copper (1083 degrees C) in approximately 7.5 seconds [6]! The via only reaches 118 degrees C because of the thermal coupling to the 2 Oz. trace.

Table 4

Temperatures for 2.5 mm trace, single via			
Current (A)	TC	Via top	Via Midpoint
7	51.3	59.0	60.8
10	93.5	113.2	117.9

Two Vias:

Even though a single via can carry significantly more current than expected, as a result of the thermal coupling to the trace, the capacity is of course greater if we use two vias. Table 5 provides the results of simulations of two 2.5 mm (100 mil) traces each with two vias. The temperatures at the two vias on each trace are virtually identical, confirming the fact that the current is splitting equally between the two vias. One trace is a 1.0 Oz trace and the other is a 2.0 Oz trace. The graphical results are shown in Figure 5. The blue lines are the via midpoint temperatures and the green lines are the trace TC temperatures.

Table 5

Temperatures for 2.5 mm trace at Various Points and Currents, Two Vias					
Weight (Oz)	Width (mm)	Current (A)	TC	Via top	Via Midpoint
1.0	2.5	6	67.1	69.5	69.5
1.0	2.5	7	88.6	92.3	92.4
2.0	2.5	6	41.3	43.3	43.5
2.0	2.5	7	49.9	52.7	53
2.0	2.5	10	89.6	96.5	97.3

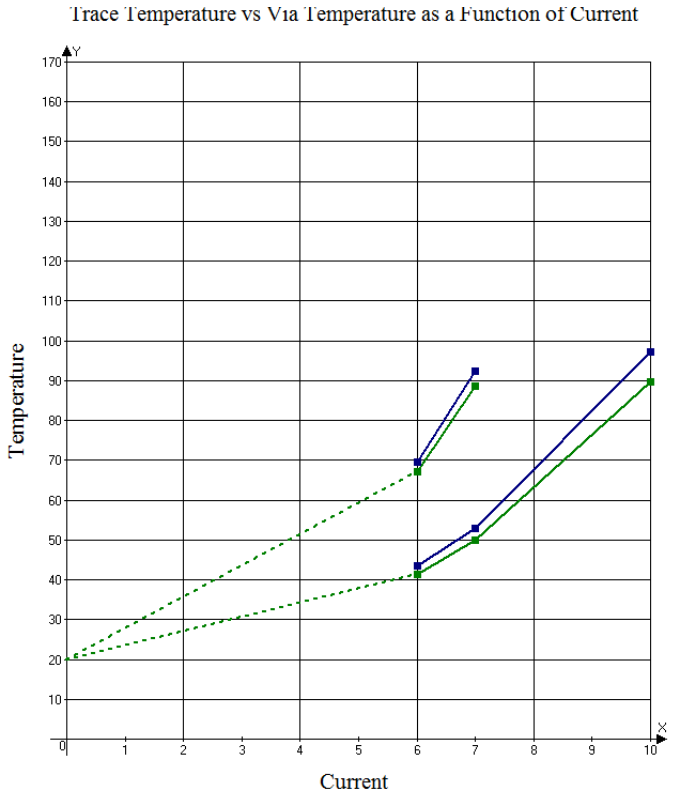

Figure 5
Trace (green) and via (blue) temperatures for a 2.5 mm trace with two vias.
The top pair of lines is for 1.0 Oz and the bottom pair of lines for 2.0 Oz. traces.

Note that even at 10 Amps through a 2 Oz. trace, the small vias are less than 10 degrees warmer than the trace.

Conclusions:

The primary conclusion from all this is that vias can carry *MUCH* more current than we have previously assumed. This explains why via failures due solely to temperature are so rare. Common wisdom has been that the via should have approximately the same cross-sectional area as the trace. For larger traces, multiple vias should be used to keep this equality. But the results from these simulations show that the following rule is approximately true instead (at least within reasonable limits):

It is not the current that determines the via temperature. The trace itself has much more influence over the via temperature..

The reader may wonder about the air filled cavity in the via core. This has no appreciable impact on via heating or cooling. The cooling of the via is through the dielectric and through thermal conductivity with the trace.

But what if we filled the via core? If we filled it with solder, there would be only a minor impact. The resistivity of solder is at least ten times that of copper, so most of the current would flow through the wall of the via anyway. Therefore, the heating and cooling characteristic would be largely the same. If we filled it with copper, the resistance would be lower so the I^2R heat generation would be less. Therefore, the thermal performance would be better. Similarly, a larger via with the same plating, or the same via with thicker plating, would also perform somewhat better.

Notes and references:

1. See Brooks, Douglas G. and Adam, Johannes, "Trace Current/Temperature Relationships", PCD&F, June, 2011, p. 22. More comprehensive analyses by the authors, "Trace Currents and Temperatures Revisited," and "Fusing Currents in Traces", 2015, are available at www.ultracad.com.
2. Throughout this paper whenever we use the term "via cross-sectional area" it is understood that we mean the "via *conducting* cross-sectional area," the cross-sectional area of the via wall.
3. TRM (Thermal Risk Management) is designed to analyze temperatures across a circuit board, taking into consideration the complete trace layout with optional Joule heating as well as various components and their own contributions to heat generation. Learn more about TRM at www.adam-research.com
4. IPC-2152, "Standard for Determining Current Carrying Capacity in Printed Board Design," August, 2009, www.ipc.org.
5. A 10 mil diameter via with a 1.0 Oz. (1.3 mil) wall has a cross-sectional area of 35.5 mil^2, equivalent to a 27.3 mil wide 1.0 Oz trace.
6. See Brooks, Douglas, and Adam, Johannes, "Fusing Currents in Traces," 2015, available at www.ultracad.com. The calculation was made with UltraCAD's UCADPCB4 Trace Calculator, available at www.ultracad.com.

About the authors:

Douglas Brooks received a BS and MS in EE from Stanford and a PhD from the University of Washington. He has spent most of his career in electronic manufacturing companies, rising from staff engineer to general manager and then president of his own company. He spent two short tours as a professor, first at San Diego State Univ. and then at the Univ. of Washington. His last 20 years were spent as owner of UltraCAD Design, Inc. a PCB design service bureau in Bellevue, WA. He has given seminars on signal integrity issues around the world, and his articles have appeared in numerous trade journals. Brooks has authored two books, the latest one, PCB Currents; How They Flow, How They React, published by Prentice Hall in 2013. He has three children and seven grandchildren, and is now retired with his wife in Kirkland, WA.

Johannes Adam received a doctorate in physics from University of Heidelberg, Germany, in 1989 on a thesis about numerical treatment of 3- dimensional radiation transport in moving astrophysical plasmas. He was then employed in software companies, mainly working on numerical simulations of electronics cooling at companies like Cisi Ingenierie S.A. , Flomerics. Ltd. and Mentor Graphics Corp. In 2009 he founded ADAM Research and does work as a technical consultant for electronics developing companies and as a software developer. He is the author of a simulation program called TRM (Thermal Risk Management), designed for electronics developers and PCB designers who want to solve electro-thermal problems at the board level. He is member of the German chapter of IPC (FED e.V.) and engages in its seminars about thermal topics. He is Certified Interconnect Designer (CID). He is living in Leimen near Heidelberg.