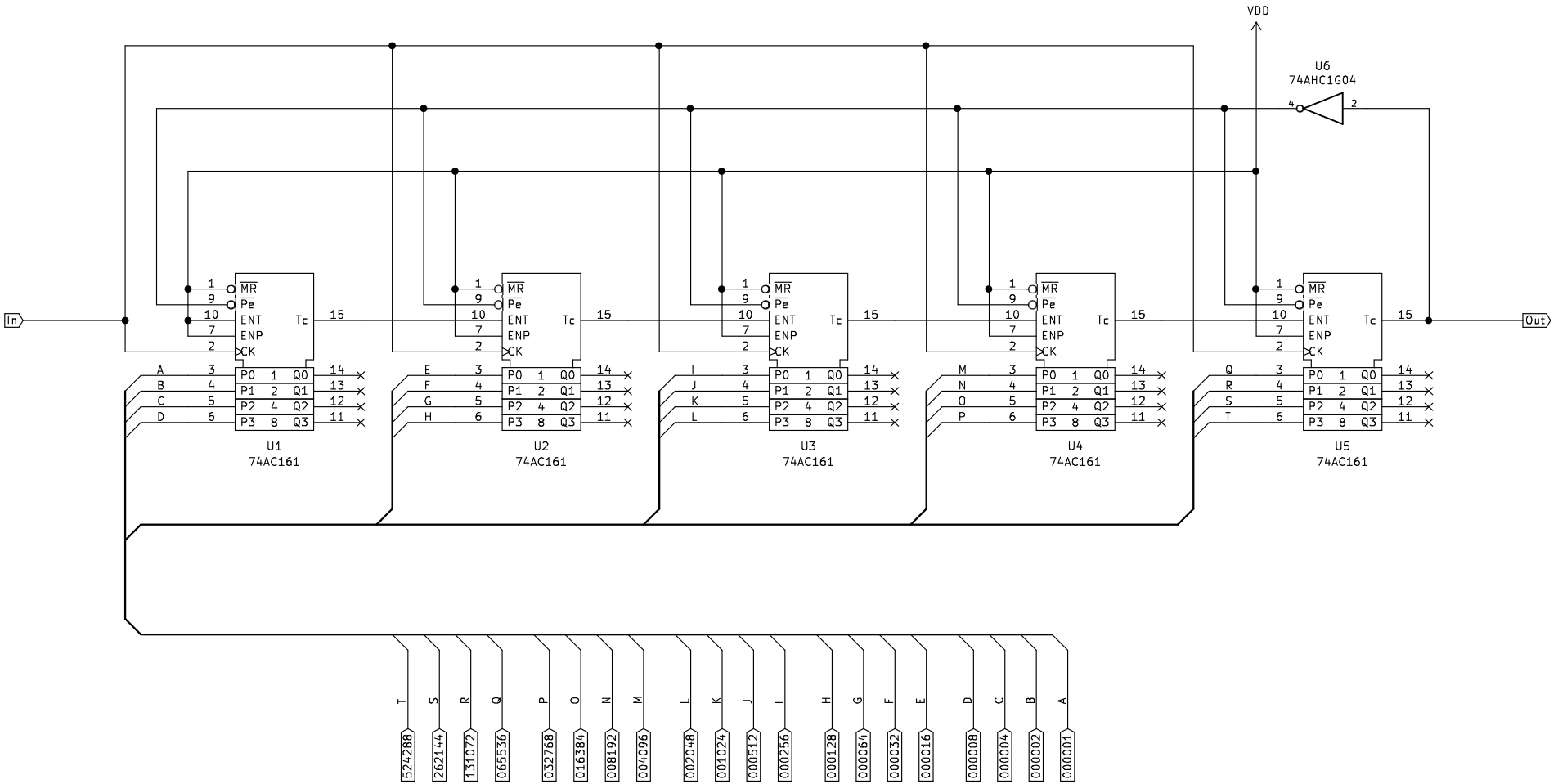

NOTES:
The input bit pattern for programming this type of divider is computed from:
16^M − N where M is the number of counter stages and N is the division ratio. In this case 1048576 − N
Minimum N is 2.

The 74AC161 alone will operate at >100 MHz, but in a cascaded divider using only ripple carry (ENT), system operating frequency will be much, much lower due to the accumulated propagation delay ENT -> TC through every counter stage.
In this circuit, maximum operating frequency is 15.48 MHz (+5 V supply voltage, worst case delay/setup timing), slower with more stages, faster with fewer.
If speed is not an issue, this design is the simplest to implement/layout (and to understand).
For higher speed, please choose my design using "Carry Look Ahead" techniques, which will run at up to 37 MHz.

For a shorter divider chain, simply remove U2, U3 or U4 from the circuit. Minimum configuration (N = 2...256) is U1, U5 and U6.

20−bit Programmable Synchronous Divider, Division Ratio: 2...1048576

Sheet: /	
File: Sync_prog_Nbit_counter_RC.sch	
Title: 20−bit−divider	
Size: A4	Date: 2020−08−01
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