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designideas

READERS SOLVE DESIGN PROBLEMS

Driver circuit lights architectural and interior LEDs

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LEDs are more efficient than incandescent lights and can last 100 times longer, but they require specialized electronic-drive circuits to avoid overstress conditions. The main operating parameter is relatively simple: Keep the current through the LEDs constant and under the specified maximum.

Traditional power supplies have accurate voltage outputs with variations in current. A resistor in series with an LED string controls the current. Such a design assumes a known voltage across the LEDs that does not vary with changes in LED temperature. Unfortunately, LEDs' forward voltage does change with temperature. LED manufacturers generally bin their devices by forward voltage, allowing a lighting manufacturer to build a lighting fixture to match this forward voltage at a fixed temperature. A circuit using unbinned LEDs saves the LED manufacturer time and results in less expensive LEDs. LEDs also have a negative forward-voltage-to-temperature coefficient that can cause the drive circuit to go into thermal runaway, requiring the designer to build safeguards into the design.

The ideal approach for driving LEDs is one in which the circuit monitors the current and keeps it constant. LEDs' forward voltage does not affect this type of circuit, eliminating the need for binning and the effect of the LEDs' negative forward-voltage-to-temperature coefficient. These circuits can be complex switching regulators or simple linear regulators with feedback loops. Complex switching regulators are ideal for high-light-output applications, such as streetlights.

Simple, economical, and robust hybrid circuits find use in architectural- and interior-lighting fixtures. These circuits' design may be less efficient than that of a complex switching regulator, but their low cost and simplicity make them attractive. These circuits operate over the full universal voltage specification of 85 to 265V ac at 50 or 60 Hz.

The circuit in **Figure 1** comprises a bridge, a chopper, and a current regulator. The full-wave bridge comprising diodes D_1, D_2, D_3, and D_4, feeds into the chopper circuit. MOSFET Q_2 immediately turns on, and capacitor C_1 begins to charge.

Resistors R_1 and R_2 form a voltage divider. When the voltage on the cathode of D_5 reaches 43.5V, the zener diode conducts and turns on Q_1, which pulls the gate of Q_2 low, causing it to turn off. Diode D_6 protects Q_2's gate.

The voltage across C_1 stays at 80 to 90V. The charge on C_1 feeds the CCR (constant-current regulator) and the LED string. This circuit example has 22 LEDs. The CCR maintains the current at 20 mA through the LED string. The circuit includes resistor R_4, in series with the LEDs, for measuring the current through the LED string.

Figure 2 shows the voltages at different parts of the cycle with an input voltage of 150V ac. Trace 1 is the output of the bridge-rectifier circuit. Trace 2 is the voltage across C_1, the output of the chopper circuit. Trace 3 is the voltage across the current-sense resistor. The traces clearly show that, when the voltage from

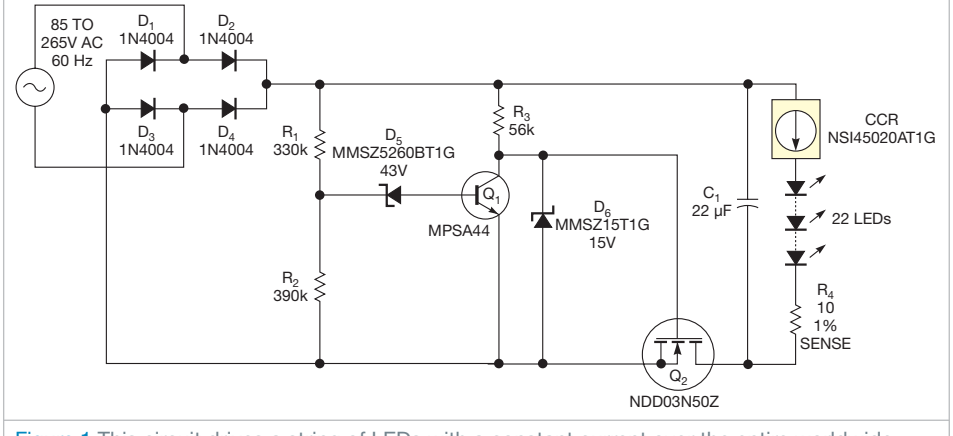

Figure 1 This circuit drives a string of LEDs with a constant current over the entire worldwide range of ac-mains voltages.

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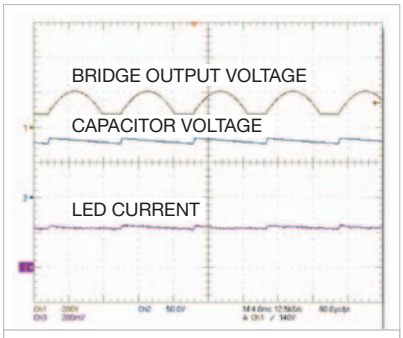

Figure 2 When the voltage from the bridge increases to more than 80V, the chopper circuit switches and limits the voltage applied to the regulator circuit.

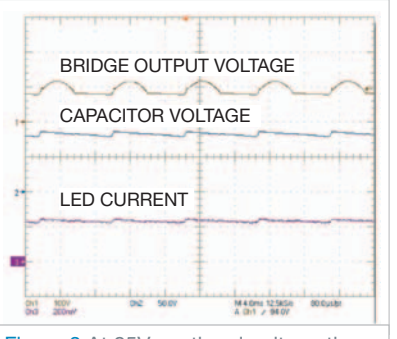

Figure 3 At 85V ac, the circuit continues to operate by keeping Q_1 on for a longer period.

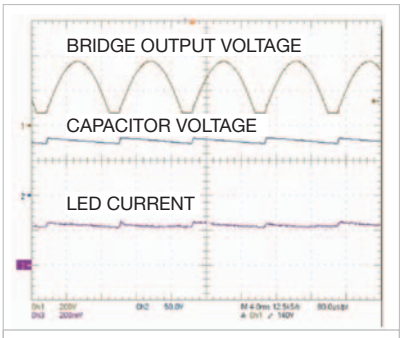

Figure 4 At 265V ac, the circuit has enough energy to keep C_1 charged during off cycles.

the bridge increases to more than 80V, the chopper circuit switches and limits the voltage applied to the regulator circuit. **Figure 3** shows the voltages with an input voltage of 85V ac.

The oscilloscope traces show that there is still sufficient design head room, with Q_1 staying on for a longer period, during which C_1 fully charges. The input voltage drops to 54V ac before the current through the LEDs begins to drop.

Figure 4 shows the circuit operation at an input voltage of 265V ac. Trace 1 shows that, because of its high input voltage, Q_1 is on for a short time. Trace 2, however, shows that sufficient energy still remains to charge Q_1 and maintain the current through the LEDs during the off cycle.

You can scale this circuit to operate with different LED arrays. CCRs are available with current ratings as high as 160 mA. For higher currents, you can place the CCRs in parallel. The values of C_1, R_1, and R_2 match the type and number of LEDs. EDN

Use op amps to make automatic-ORing power selector

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Many systems must select among two or more low-voltage dc-input sources, such as an ac adapter, a USB (Universal Serial Bus) port, or an onboard battery, for example. You can implement this selection using manual switches, but automatic switching is preferable. You usually want to use the highest-available input voltage to power your system. You can accomplish this task using a Schottky-diode ORing scheme (**Figure 1**). Unfortunately, the forward-voltage drop of a Schottky diode ranges from 300 to 600 mV. This voltage wastes power, creates heat, and decreases the voltage available to your system.

Efficient voltage ORing requires only a P- or an N-channel MOSFET, a suitable op amp, and a few passives. This Design Idea describes the application of voltage ORing to positive dc-power rails. The P-channel-MOSFET design is suitable for low-power, single-supply systems operating at 3.3V or higher, and the N-channel MOSFET fits situations in which the bus voltage is lower or the current is higher and a suitable op-amp bias voltage is available.

Positive current flows from the MOSFET drain in an N-channel-FET design. In a P-channel design, the current flows from the MOSFET source. The MOSFET's drain-body diode would defeat rectifier operation if the usual current flow (for switching or amplification) were used.

Your first design task is to choose a suitable MOSFET. The MOSFET's worst-case on-resistance must be low enough so that the I×R (current-times-resistance) drop with full-load current is low enough to accomplish the design objectives. A 0.01Ω MOSFET has a 50-mV forward-voltage drop when 5A flows through it. Be sure to consider power dissipation due to $R \times I^2$ and the resulting temperature rise.

Your second design task is to choose an op amp. The op amp must be able to operate with the voltages involved and to adequately drive the MOSFET's gate voltage. The P-channel design requires a rail-to-rail I/O type. A single-supply op amp is adequate for the N-channel design. Another important consider-

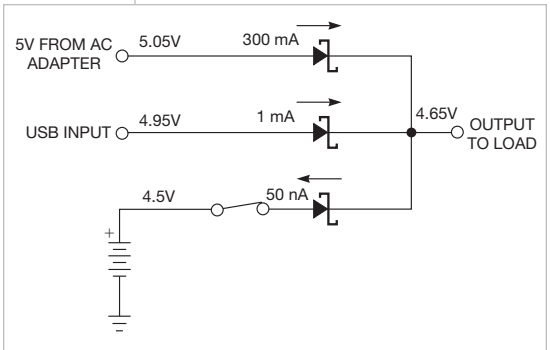

Figure 1 Schottky-diode ORing can power a load from the highest input-voltage source.

ation is the op amp's input offset voltage, V_{OS}. The total $\pm V_{OS}$ window must be less than the maximum desired voltage drop across the MOSFET. For example, if you permit a 10-mV forward-voltage drop at full load, then the op amp should specify an offset voltage of ±5 mV or better.

R_1/R_2, R_{11}/R_{12}, and R_{21}/R_{22} form the input-voltage divider, which biases the op-amp input at a level slightly below that of the input voltage that it is controlling (**figures 2** and **3**). This offset must exceed the op amp's maximum offset voltage to ensure that all op-amp parts in production always turn off the MOSFET when you apply reverse voltage. In the example of the P-channel 5V design, R_1 and R_2 bias the inverting op-amp input at 99.9% of the input voltage, or 4.995V dc. In steady-state operation, the op amp servos with the conducting MOSFET to keep the other op amp's input at the same voltage, within the tolerance of the op amp's offset voltage. With a perfect 0V-offset op amp, light-load currents cause the MOSFET to only partially enhance, so the circuit delivers a 5-mV MOSFET forward-rectifier drop. This mild effect is the only disadvantage of R_1 and R_2's input offset biasing. If the MOSFET resistance is too high to allow it to maintain 5 mV at full load, then the op amp fully enhances the MOSFET as its output swings to the rail, and the ORing circuit delivers the MOSFET's fully enhanced on-resistance.

You can consider the MOSFET's variable on-resistance as the element with which the op amp senses current. When you apply reverse voltage, the MOSFET de-enhances, the I×R voltage drop increases, and the op amp's output ends up at the appropriate supply rail, driving off the MOSFET as hard as it can.

With light-load conditions and a given offset voltage, the op amp tries to servo the voltage on its power-output-sensing input to the voltage on its power-input-sensing input plus the offset voltage. With R_2 open-circuited, the op amp has no intentional external offset. If the op amp's offset voltage were in the unfavorable direction, a sizable reverse-cutoff current would occur if the input-power bus were to fall to a lower potential than the output-voltage bus.

Figure 4 shows current-voltage test data for the operating region. The complete design, including intentional offset, produces the green curve. The

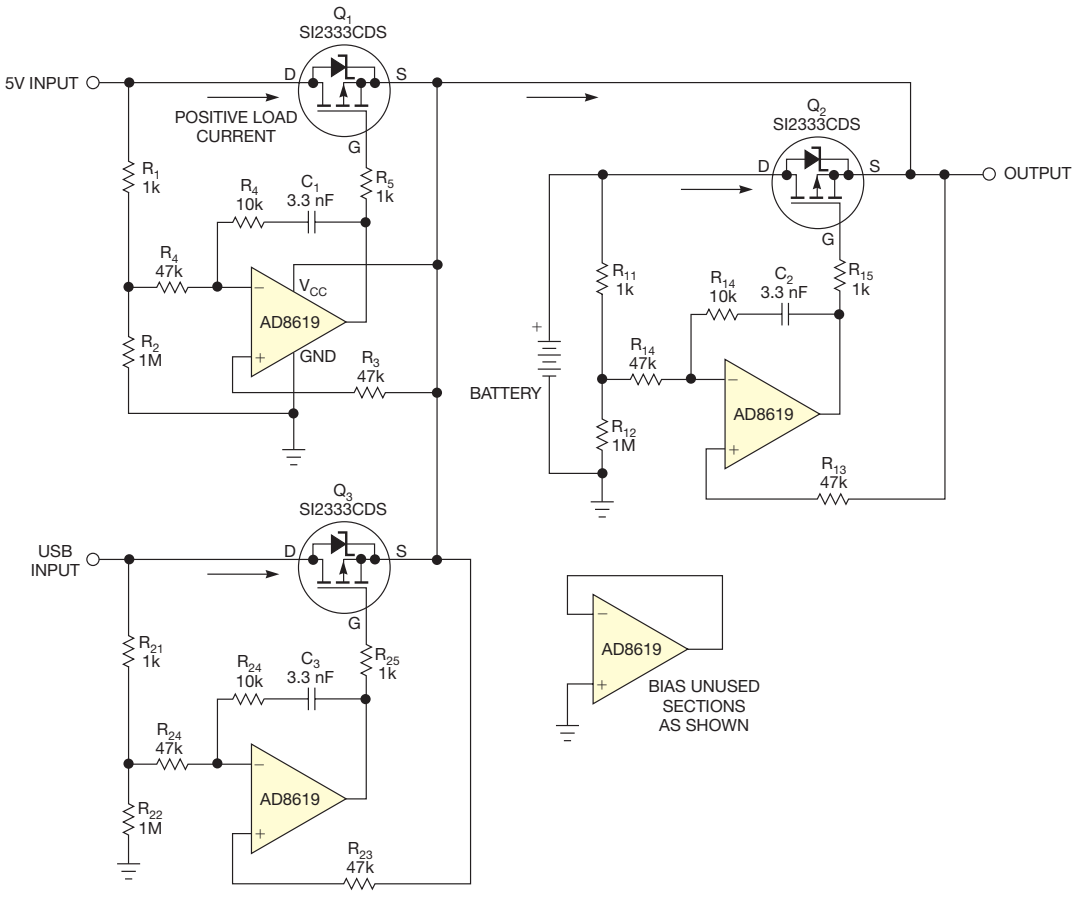

Figure 2 MOSFET power ORing using P-channel MOSFETs is the more common choice for single-rail systems when the rail voltage is sufficient to operate the op amp and drive the MOSFET gate.

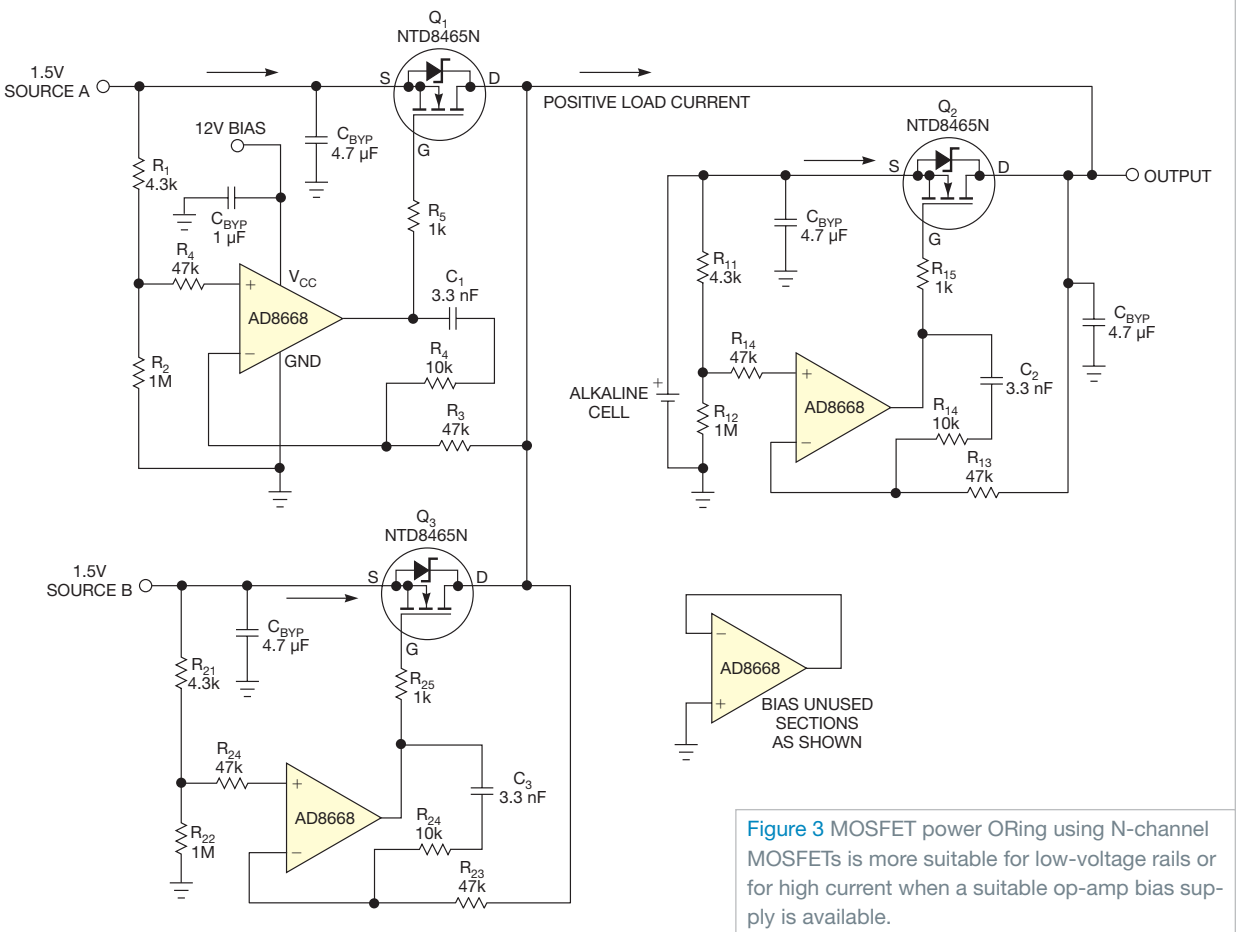

Figure 3 MOSFET power ORing using N-channel MOSFETs is more suitable for low-voltage rails or for high current when a suitable op-amp bias supply is available.

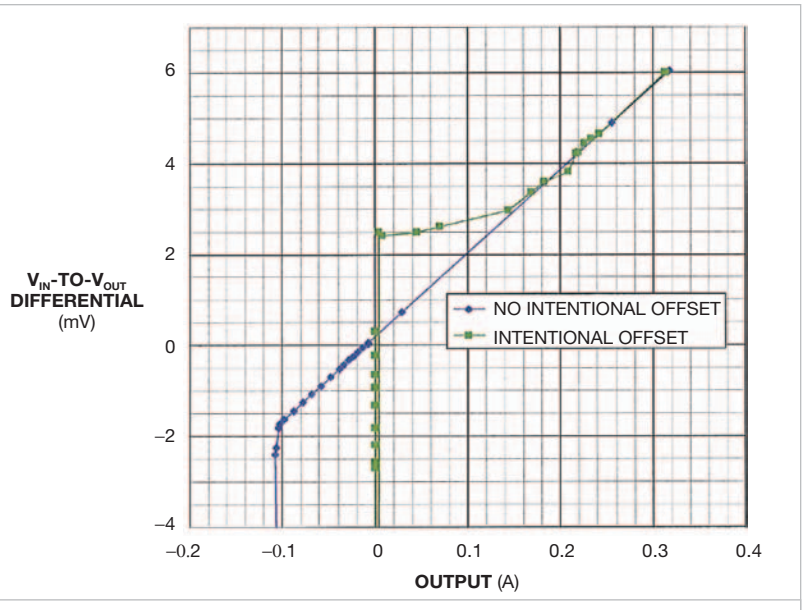

Figure 4 The green curve shows results with the correct external offset applied. The blue curve shows results when the op amp's internal offset is in the unfavorable direction and no external offset is applied.

equivalent of an unfavorable internal offset and no intentional external offset produces the blue curve. Although the green curve sacrifices some forward-voltage drop at light-load conditions, its forward voltage is always less than the full-load maximum. The intentional offset avoids any significant reverse current in the MOSFET. This design can switch at the 0A current transition, at which the leakage-current MOSFET's drain-body diode is likely to dominate.

On the other hand, the blue curve, without intentional offset, permits significant reverse current under some circumstances. This example shows approximately 100-mA reverse current with 2-mV reverse voltage across the MOSFET before the circuit switches off the MOSFET. Both the P- and the N-channel designs have undergone testing, and the P-channel design is in production. EDN

Charging time indicates capacitor value

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A recent research project using a capacitive sensor to measure water levels comprises two PCB (printed-circuit-board) plates placed one in front of the other at a controlled distance. Every plate divides into eight equal copper zones, resulting in eight equivalent parallel-plate capacitors (**Figure 1**). Every capacitor has a plate area of 25 cm^2. To measure the water's total height, the project uses a special hydro-insulated layer to avoid short circuits. Knowing the layer thickness and the electrical permittivity of the hydro-insulated substance allows you to express the distance between every two plates and the dielectric's electrical permittivity.

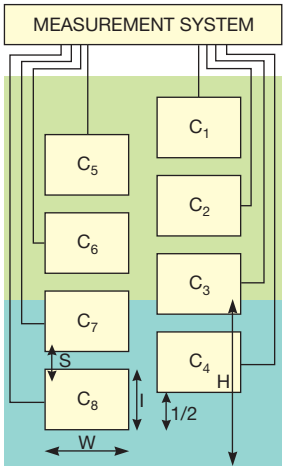

Figure 1 Plates and a PCB's dielectric form a capacitor bank for measuring water level.

The capacitance of every two overlapped copper zones can vary only when the electrical permittivity changes because all other parameters—the plate's area and the distance between the plates—are constant, as the following **equation** shows: $C_X=(\varepsilon_0\varepsilon_R A)/D$, where $\varepsilon_0=(8.854\times10^{-12})$F/m, the void electrical permittivity, ε_R is the dielectric's relative electrical permittivity, D is the total dielectric thickness, C_X is the capacitance of the measured capacitor, and A is every plate's surface. The relative electrical permittivity strictly depends on which and how many materials are between the capacitor plates. This application uses four kinds of ε_R: air, air-hydro-insulated varnish, water-hydro-insulated varnish, and air-water-hydro-insulated varnish. At this point, you must consider the capacity of the capacitors at the surface-separation line between air and water.

To measure capacitance and thus measure the water level, a measurement system employs a 20-MHz ATTiny 2313 microcontroller and a fast LT1016 analog comparator (**Figure 2**). The measurement algorithm uses the microcontroller's OC1A and OC1B output-comparator signals. The ATTiny 2313 sets both pins at once but to opposite values. When OC1A is 5V, you can simultaneously set OC1B using assembly-language code. The same situation occurs when OC1B is 5V; OC1A is then 0V. In the first case, the quantity of the charge rises on the first plate and lowers on the other plate. Reversing the polarity causes the second plate to acquire more charge, and its potential rises. When both plates have the same potential, the LT1016 comparator enables the ICP pin on the microcontroller, saving the number in the internal timer counter and sending it through the serial port for further processing. When the voltages on both plates are equal, the voltage on the capacitor is halfway from the input signal's amplitude, $V_{CC}/2$.

The pulse width of both OC1A and OC1B must be larger than the maximum capacitor's charging time, which you obtain when you measure the water's dielectric capacitor, according to the following **equation**: $PW\geq10\times R_e\times C_{MAX}$. **Figure 3** shows the waveforms.

The charging **equation** in the transient region is:

$$\frac{V_{CC}}{2}=V_{CC}+[0-V_{CC}]e^{-\frac{t}{2RC}}\Rightarrow\frac{1}{2}=e^{-\frac{N_1 t_{CLK}}{2RC}}.$$

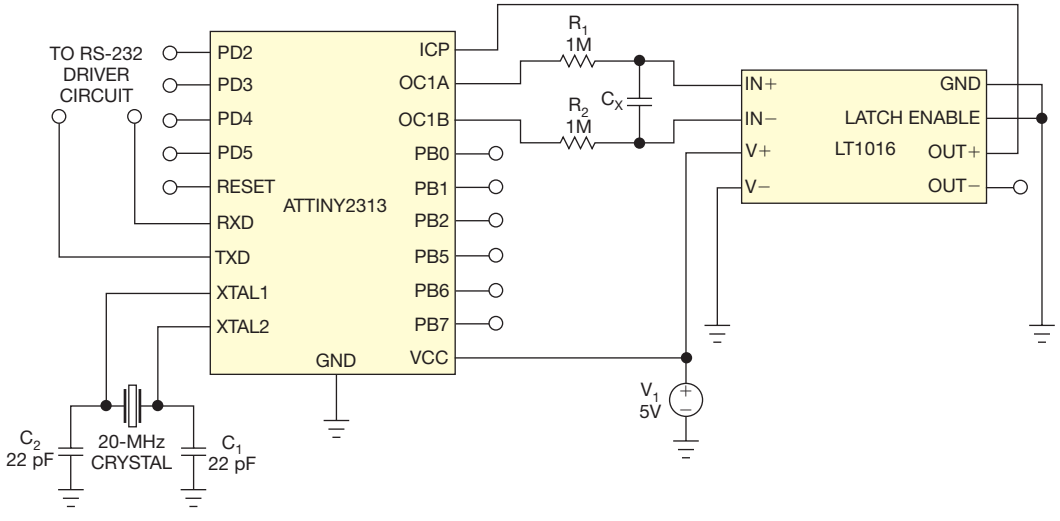

Figure 2 The measurement circuit comprises an ATTiny 2313 microcontroller and a comparator.

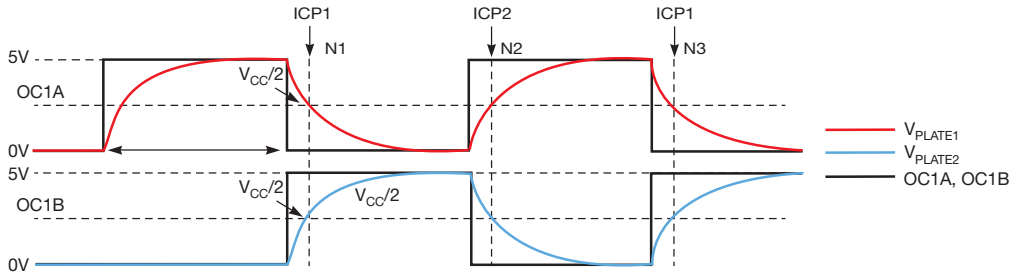

Figure 3 The capacitor plates have equal voltages at $V_{CC}/2$.

You can then extract the capacitance using the following **equation**:

$$C_x=\frac{N_1 t_{CLK}}{2R\ln 2},$$

or

$$C_x=0.036067376\times N_1 \text{ pF}.$$

You can extract the level on both the left and the right side of the capacitive sensor in **Figure 1**, resulting in two **equations** but the same result. The algorithm consists of first measuring all the capacitors—completely immersed, partially immersed, and nonimmersed—and then expressing the surface of both C_7's and C_3's capacitor plates at the surface-separation line, using the unknown H variable. You then extract the unknown value of the level, obtaining both capacitive-dependent **equations**:

$$H=f\left(\frac{C_{PARTIALLYIMMERSED}}{C_{NONIMMERSED}}, L, \varepsilon_{AIR}, \varepsilon_{LAYER}, \varepsilon_{WATER}, D_{AIR}, D_{LAYER}\right).$$

From the capacitive-measurement-procedure point of view, the designed system represents a floating measurement method that implies two similar parallel-plate armatures. This method halves the parasitic capacitances that occur during measurement referred to system ground. EDN